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Deep Levels in Ion Implanted GaAs

Final Report

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December 1985

INTRODUCTION

There are major GaAs digital and analog technologies built around selectively ion implanted field effect transistors (FET's). Despite the impressive success of ion implantation in these technologies, it has not attained the level of application in the III-V's that it has in Si. This is in part because of the prevailing attitude that ion implantation cannot be used to fabricate devices in the III-V's that are sensitive to defects. The situation is similar to that which existed in the Si community some years ago, when it was widely held that bipolar transistors could not be made by ion implantation because of the residual damage and its effect on device performance. Today, it is generally accepted that it is not possible to make III-V mixer diodes, buried channel CCD's or laser diode ohmic contacts by direct ion implantation. It is the premise of this program that the information upon which to make such a judgement is not available, and that in fact, the prevailing wisdom may well be wrong. The goal of the program is to establish the 'intrinsic' limitations on the use of ion implantation in GaAs by measuring the bulk traps which are unambiguously associated with the implantation process.

This study is of interest to NRL at this time, because of the major improvements which have recently occurred in bulk LEC GaAs material and the advent of MeV implantation. NRL has made layers with carrier concentrations on the order of $1X10^{16}$ cm^{-3} and mobilities of 6700 cm^2/Vs by direct ion implantation of bulk LEC GaAs substrates. Commercially available MeV accelerators, instrumented for ion implantation allow one to make doped layers in excess of three micrometers thick, and NRL has shown that it is possible to use MeV implantation in conjunction with the improved substrates to make device quality layers of a type appropriate to the fabrication of a new family of devices. A detailed study of the traps associated with these low level

implants is critical at this time as an aid in the application of MeV implantation to the fabrication of these new devices.

BACKGROUND

There is a substantial literature on the use of Deep Level Transient Spectroscopy (DLTS) in GaAs for the characterization of the majority carrier traps which are produced during ion implantation and subsequent annealing.[1-6] Optical DLTS (ODLTS) has also been used, but to a much smaller extent, to study minority carrier traps.[1,3,6] An excellent summary, for the purpose of this study is given by Martin and Makram-Ebeid in Ref. 6. A second relevant paper by Martin et al is Ref. 3, which discusses compensation mechanisms in Boron implanted GaAs. The distillation of these studies is that, for ions as light as B, low dose (less than $1X10^{12}$ cm^{-2}) implants show no measurable residual defects after anneals of 350 to 550°C, except in the near surface region. Higher dose implants of B show complex damage spectra which result in defects which cannot be annealed out at 550°C. The evidence is that, at least for light ions and for implant levels less than $1X10^{13}$ cm^{-2}, the implantation induced damage can be annealed out by conventional processing. However, under all conditions a damaged surface layer still exists. Furthurmore, the work of Jervis, Woodward and Eastman Ref. 1 suggests that even for ions as heavy as Si all the implantation induced traps can be removed by conventional processing (for low implants) although they too see a residual surface layer of traps.

The issues being addressed by this program are: to what degree can the implantation induced traps associated with Si implantation be removed by annealing, to what degree is residual surface damage a problem and what is the total trap spectrum, i.e., what are the trapping levels in the top and bottom halves of the bandgap. A varied approach has been laid out to meet these objectives.

APPROACH

The bulk of the work to date has employed surface Schottky barrier diodes as the basic test structure for the DLTS measurements. This structure makes it impossible to profile the entire implanted region. In addition, the low Schottky barrier height on p type GaAs makes it difficult to get information on p type material. To avoid these problems, and to increase the utility of the test structure, we have acquired material which is p+/p/n+/SI substrate and the analogous n+/n/p+/SI substrate which can be fabricated into pn+ or np+ junction test structures. Because of this unique test structure the DLTS and ODLTS measurements, are able to profile trap spectra from the substrate to the surface. Since the implanted layer is approached from the back side it is possible to avoid the residual surface damage. The use of p+/p/n+ and n+/n/p+ structures allows one to get a measure of the traps generated in both the upper and lower halves of the bandgap. In addition the optical stimulation used in ODLTS experiments allows the measurement of minority carrier traps in both the n and p layers. A comparison of the results obtained in these two manners gives one a measure of the effect of the position of the Fermi level on the residual trap spectrum.

EXPERIMENTAL

A computer controlled measurement system was used to obtain the DLTS and C-V results presented here. The system is equipped with a Boonton capacitance meter, a Lake Shores Cryotronic temperature controller, a pulser for supplying excitation voltages, and an infrared LED for optical excitation. The computer has several digital to analog converters for providing DC bias voltages, and a fast analog to digital converter which is multiplexed in order to measure several analog signals. A digital output board in the computer is used to provide trigger pulses to the boxcar and the excitation sources.

Conventional boxcar DLTS measurements are carried out by applying the Boonton's output to a dual channel boxcar which measures the difference between the capacitance at times T_1 and T_2 as the temperature is swept.[7,8] The computer controls the rate of change of the temperature while it records the boxcar's output and the temperature. This arrangement is used to measure capture rate, or defect concentration profile data which only require recording one spectra for each bias or excitation pulse width. Activation energy data are obtained by digitizing the capacitance transient output of the Boonton after each excitation pulse. Signal averaging is carried out by measuring many transients at a fixed temperature and then averaging them. This process is repeated at many temperatures in order to obtain the data necessary to produce simulated boxcar spectra by a computer program. Because the entire transient is recorded, it is possible to generate the spectra for many different emission rates in one temperature sweep.

Defect activation energies, E_a, are found by using a least squares technique to fit

$$\varepsilon = AT_p^2 \, e^{-E_a/K_B T_p} \qquad (1)$$

where ε is the emission rate the system is tuned to detect, T_p is the temperature at the peak of the DLTS line, and K_B is the Boltzmann constant. A is a constant which depends on the density of states at the band edge, the capture cross section and the thermal velocity.

Majority carrier trap spectra are studied by applying a quiescent reverse bias to the diode and then pulsing it to zero bias to fill the traps. Filling pulses from 2 to 200 microseconds long with heights from 0.5 to 10 volts are provided by a pulse transformer driven by a Systron Donner pulser. Minority trap sectra are obtained by irradiating the sample with light from an IR emitting LED at wavelengths of either 880 nm or 940 nm which correspond to

energies just below the bandgap for GaAs. For light pulses about 10 microseconds long, the LEDs are driven with up to 8 A currents which corresponds to a light power of about 40 mW. The current is reduced substantially to prevent damage to the LEDs when longer pulses are used. In the latest measurement system the LED is held at room temperature and a quartz light pipe is used to couple light to the back side of the device. The first ODLTS experiments were done with the LED mounted near the front surface of the sample. Therefore, the LED's temperature and its light output varied during the temperature sweep. This system is no longer used as it is difficult to incorporate the variations in the LED's light output into an analysis of the DLTS results.

C-V measurements were also made at several temperatures with the computer controlled system as these results are necessary to obtain quantitative information on defect concentrations. The data were analyzed to determine the carrier concentration, n_s, vs depth, d, using

$$d = \varepsilon_s / C \tag{2}$$

$$n_s = 2/q\varepsilon_s \frac{d}{dV} \frac{1}{C^2} \tag{3}$$

where ε_s, C, q, and V are the dielectric constant, capacitance, electronic charge, and bias respectively. The free carrier concentration vs depth data also reveal useful information about carrier removal.

The DLTS analysis uses the capacitance, C_o, at the quiescent reverse bias and the free carrier concentration to obtain trap concentrations, N_T , from

$$N_T = f\, n_s\, \Delta C / C_o \tag{4}$$

where ΔC is the amplitude of the DLTS peak. f can be evaluated by using Poisson's Equation to calculate DLTS lineshapes. In general, f depends upon the quiescent reverse bias, pulse height, Fermi energy, free electron concentration, and the energy of the trap. These calculations were carried out for the data presented here, and f was found to vary from 5 to 15.

It is not possible to obtain quantitative results for the minority carrier trap concentrations from the ODLTS data presented here, because the light intensity was too weak to saturate the traps. In addition, a quantitative analysis of ODLTS data requires a knowledge of the photoionization cross sections and the thermal emission rates for electrons and holes on the defect, and these have not been measured.[9,10] An effort has been made to be systematic when making the ODLTS measurements so the peak intensities can be used to set lower limits on the minority trap concentrations even though absolute values are unknown.

Schematics of the np+ and Schottky barrier samples are diagramed in Fig. 1. The np+ diodes were produced by MBE by first growing a one micrometer thick p+ layer containing ~$1X10^{18}$ Be cm^{-3} on a semi-insulating GaAs substrate. This was followed by a Si doped layer about two micrometers thick. C-V data on the as grown samples indicate a free carrier concentration of $5X10^{15}$ cm^{-3}. The Schottky barriers were grown on an approximately 10 micrometer thick n-type LPE layer which was doped with Sn to a free carrier concentration of $9X10^{16}$ cm^{-3} as measured by C-V. The np+ samples and Schottky barriers were studied as grown, annealed but not implanted, as well as implanted and annealed. The Schottky samples were used to study the dependence of the defects on the thickness of the cap layer and the annealing temperature. All the samples were capped with a Si_3N_4 layer during the annealing stages.

RESULTS

C-V data for the as grown, annealed, as well as the implanted and annealed np+ samples are shown in Fig. 2a, and the carrier concentrations deduced from the data are shown in Fig. 2b. The free carrier concentration for the as grown sample is uniform through out the layer which is expected from the growth conditions. The carrier concentration for the annealed sample

is considerably smaller than that for the as grown material and it varies with depth. This indicates that defects which compensate GaAs were introduced during the annealing. The implanted and annealed sample has a carrier concentration which increases with distance on going away from the np+ junction. The peak in the carrier concentration is located near where the peak in the concentration of the implanted ions is expected to be. The sharp decrease in the number of free carriers beyond the peak suggests an increase in the number of compensating defects on approaching the surface. The spacial dependence of the free carrier concentration in this compensated region is not an accurate representation of the actual concentration in the sample, as the simple C-V analysis used here does not consider that the Debye length increases with decreasing concentration. The sharp decrease in the carrier concentration near the top surface of the sample is also seen in the capacitance data as a step decrease at high bias. The C-V results for the annealed sample have a similar step but at a lower voltage. This is reasonable as the implanted sample has a higher carrier concentration and thus a shorter depletion width than the annealed sample.

The majority carrier DLTS spectra for these samples is shown Fig. 3. The data reported here are values of $n_s \Delta C/C_0$ which is related to the defect concentration by Eq. (4). Since all the data here have nearly the same value of f, these curves can be used to compare relative trap concentrations. The spectrum for the as grown material contains a pair of nearly overlaping lines which are quite different from the lines for the other samples. The spectra for the implanted and annealed sample is shifted slightly in temperature from that for the annealed sample, but both lines are believed to be due to the same defect. The shift is believed to be due to a measurement phenomena as the activation energy varried between 0.24 and 0.34 eV depending on the

reverse bias, pulse height and the pulse width. The importance of the results presented here is that the implanted and annealed sample does not contain any DLTS lines not already present in the annealed control sample. To determine whether there is a significant difference in intensity between the annealed control sample and the implanted and annealed sample, several diodes of each type were measured with a number of different quiescent reverse biases. These results are presented in Fig. 4 where the peak values of $n_s \Delta C/C_o$ is plotted against the bias. These results indicate that the concentration of the 0.3eV defect in the implanted samples is at most two times larger than the concentration of the 0.3 eV trap in the annealed diodes. Values of E_a=0.34 eV and $A=1x10^7$ sec $^{-1}$ K^{-2} were used with an average free carrier concentration of $4x10^{15}$ cm^{-3} and trap concentrations $N_T=1x10^{15}$ cm^{-3} and $1.6x10^{15}$ cm^{-3} to predict the model peak intensities also shown in Fig. 4. This modeling suggests there may be a slight increase in the defect concentration on approaching the surface, as the model with $N_T=1x10^{15}$ cm^{-3} gives a good fit to the low bias experimental data, and using $N_T=1.6X10^{15}$ cm^{-3} gives a reasonable fit to the high bias results.

Minority carrier trap spectra for an annealed and for an implanted and annealed sample are shown in Fig. 5a for a reverse bias of 1 volt. The data reveal a broad low temperature peak with $n_s \Delta C/C_o$ ~$8X10^{12}$ cm^{-3}, which corresponds to a minimum defect concentration of $8X10^{13}$ cm^{-3}. The ODLTS data contained no lines at higher temperatures. Data acquired with a lower light intensity indicate that this line is composed of the spectra for several defects. The ODLTS spectra recorded at higher biases are plotted in Fig. 5b for these two samples. The intensity of the lower temperature peaks is smaller here than in Fig. 5a, but more importantly, a large peak with a trap concentration of at least $5X10^{14}$ cm^{-3} is found at higher temperatures. The

intensity of this peak increased dramatically for biases near the knee in the C-V data in Fig. 2. This line was also measured with several light intensities and it is not saturated. At low light intensities, the peak split into two indicating the presence of several different traps. These ODLTS results suggest that the annealing introduced a high concentration of traps in the lower half of the bandgap near the sample's surface.

A number of Schottky barrier samples were grown on LPE GaAs to study the effects of the capping and annealing on implanted and unimplanted GaAs. The as grown LPE layers typically contained fewer than 10^{14} cm^{-3} electron traps as illustratedby the spectra in Fig. 6a. ODLTS spectra were measured with the older optical excitation system with the infrared LED mounted near the front surface of the sample. Fig. 6b illustrates that the ODLTS measurements on the as grown LPE samples showed no evidence of any minority carrier traps, which is expected for good LPE GaAs. DLTS measurements made after implanting samples with $1X10^{11}$ Si cm^{-3} and annealing them at 800°C for 20 minutes with a Si_3N_4 cap, indicate the presence an electron trap with an activation energy of 0.72 eV as shown in Fig. 6c. The shoulder on the low temperature side of the peak indicates the presence of a second trap with a smaller activation energy. The narrow lineshape indicates that the spectra is due to a simple point like defect. After stripping off the Sckottky, about 0.2 micrometers of the GaAs was etched away, and new Schottky barriers were fabricated. The DLTS spectra in Fig. 6d for these new diodes contains a less intense line at 0.72eV as illustrated by the data in Fig. 6d. This test shows that the concentration of the 0.72eV defect is higher at the surface than in the bulk, but it does not determine whether the defect was produced by the ion implantation or the annealing. The ODLTS spectra in Fig. 6e was recorded after the etching process, and it indicates the presence of a number of minority carrier traps.

The defects introduced by annealing at 850°C for 20 minutes while using a Si_3N_4 cap are illustrated by the data in Fig. 7. Several cap thicknesses were used since the stress induced by thermal expansion on annealing may be in part responsible for producing defects. In general, these cap thicknesses are greater than those normally used in device processing as the study here is interested in determining the posibility of a dependence on the cap thickness. After capping and annealing, all the samples had electron trap concentrations less than 10^{14} cm^{-3} as illustrated by the data in Fig. 7a, which was measured for a sample capped with 0.25 micrometers of Si_3N_4. The hole trap spectra for samples with 0.046, 0.17 and 0.25 micrometers thick caps are shown in Figs. 7b, 7c, and 7d, respectively, and they indicate a significant increase in the concentration of the traps as the thickness of the cap increased. The lines in Figs. 7b, 7c and 7d are broad compared to those expected for simple point defects, indicating that the capping and annealing introduced complex defects.

CONCLUSIONS

The advantages of using a burried np+ structure to study the defects produced by ion implantation are demonstrated by the data presented here. Because the np+ junction is deep inside the GaAs, the low bias C-V, DLTS and ODLTS data reflect the carrier and trap concentrations on the back side of the implanted regions. A quick inspection of the DLTS and ODLTS results at low bias reveals that, in the vicinity of the np+ junction, the implanted sample contains the same majority and minority carrier traps as the annealed control sample. The ODLTS results at high bias indicate the presence of minority carrier traps near the surfaces of both the samples, and that the concentration

of these traps increases on approaching the surface. The C-V and carrier concentration data also indicate that the processing has resulted in a large carrier removal near the surface of the implanted and the annealed control samples. The similarity of these surface results suggests that the capping and annealing is responsible for the surface damage. If these tests were carried out with Schottky barriers on the surface of the n-type GaAs, all the spectra would contain peaks due to the surface damage produced by the annealing, and it would be difficult to draw any conclusions about how much of the damaged was induced by the ion implantation.

Low bias DLTS measurements were carried out on the np+ samples over a broad temperature range in order to probe for traps from mid gap to about 0.1 eV below the conduction band. The data in Fig. 3a shows that both the implanted and the annealed control np+ junctions contain only one majority carrier trap with a concentration greater than $1X10^{13}$ cm^{-3}. Fig. 4 reveals that the concentration of this majority carrier trap is larger in the implanted sample than in the annealed control one. The results of a lineshape calculation using the experimentally measured carrier concentration and trap parameters are also plotted here to indicate that the trap concentration in the implanted device increases on approaching the surface. Fig. 4 contains data taken at a bias near the knee in the C-V data, but the peak shows no sign of a change in its concentration at these biases as seen for the high temperature peak in the minority carrier spectra.

The ODLTS experiments cannot be used to determine an upper limit on the number of defects in the lower half of the band gap, but a comparison of the spectra in Figs. 4a and 4b indicate that the same traps are found in the implanted and the annealed control samples. The rapid increase in the intensity of the high temperature ODLTS peak occurs near the bias where the capacitance

decreases suggesting that this trap may be in part responsible for compensating the surface. The similarity of the data for the implanted and the annealed samples indicate that these traps are produced by the capping and annealing.

The data in Figs. 6 and 7 which was obtained for Schottky barriers on LPE GaAs emphasizes the need to investigate the capping and annealing furthur. Only the spectra in Figs. 6c and 6d contained a majority carrier trap after implanting and annealing at 800°C. A similar trap was not found in the implanted np+ samples or the Schottky samples annealed at 850°C. The results on hand, cannot be used to determine whether this 0.72 eV trap was produced by the ion implantation and diffused to the surface on annealing or whether it was produced by annealing alone. It's absence in the data for samples annealed at 850°C indicates that this is a better annealing temperature than 800°C for removing this trap.

In summary, the DLTS measurements have not found any majority carrier traps with a concentration greater than 1×10^{13} cm^{-3} after annealing an implanted sample at 850°C. The implanted and annealed samples were found to have the same minority carrier trap spectra as the capped and annealed control samples. The capping and annealing results point out the need to investigate other methods such as rapid thermal annealing and capless annealing in order to prevent surface damage on annealing.

REFERENCES

1. T.R. Jervis, D.W. Woodward, and L.F. Eastman, Electron. Lett. 15, 619 (1979).

2. K.L. Wang, G.P. Li, P.M. Asbeck, and C.G. Kirpatrick, Defects in Semiconductors (North-Holland Inc.), 487 (1981).

3. G. M. Martin, P. Secordel, and C. Venger, J. Appl. Phys. 53, 8706 (1982).

4. G.P. Li and K.L. Wang, J. Appl. Phys. 53, 8653 (1982).

5. M. Taniguchi and T. Ikoma, Inst. Phys. Conf. Ser. 65, 65 (1983).

6. G.M. Martin and S. Makram-Ebeid, Physica 116b, 371 (1982).

7. D.V. Lang, J. Appl. Phys. 45, 3014 (1974).

8. G.L. Miller, D.V. lang, and L.C. Kimerling, Ann. Rev. Mater. Sci. 1977, 377 (1977).

9. A. Mitonneau, G.M. Martin, and A. Mircea, Inst. Phys. Conf. Ser. No. 33a, 73 (1977).

10. B. Hamilton and A.P. Peaker, J. Appl. Phys. 50, 6373 (1979).

FIGURE CAPTIONS

Fig. 1. Schematics of the np^+ devices grown by MBE, and the Schottky barrier on LPE GaAs samples.

Fig. 2. (a) capacitance vs voltage data for np^+ samples as grown, annealed, and implanted and annealed. (b) the free electron concentration vs depth calculated from the data in (a).

Fig. 3. DLTS data for np^+ samples as grown, annealed, and implanted and annealed. The baselines have been offset vertically.

Fig. 4. $n_s \Delta C/C_o$ vs bias for np^+ devices: + annealed and • implanted and annealed. The solid and dashed lines were calculated from a model using $N_T=1x10^{16}$ and $N_T=1.6X10^{16}$ cm^{-3} respectively.

Fig. 5. ODLTS minority carrier trap spectra for np^+ junctions: (a) annealed as well as implanted and annealed measured with a reverse bias of one volt; (b) reverse bias of six volts for the annealed sample and seven volts for the implanted and annealed device.

Fig. 6. Spectra for Schottky diodes on LPE GaAs: (a) majority carrier trap DLTS and (b) minority carrier ODLTS on the as grown LPE GaAs. (c) DLTS for an implanted and annealed LPE sample. (d) DLTS and (e) ODLTS after etching off 0.2 micrometers of the LPE surface.

Fig. 7. Spectra for LPE GaAs annealed at 850°C for 20 minutes with a variety of Si_3N_4 cap thicknesses: (a) DLTS for a 0.25 micrometer cap; (b), (c), and (d) ODLTS for samples with 0.046, 0.17, and 0.25 micrometer thick caps respectively.

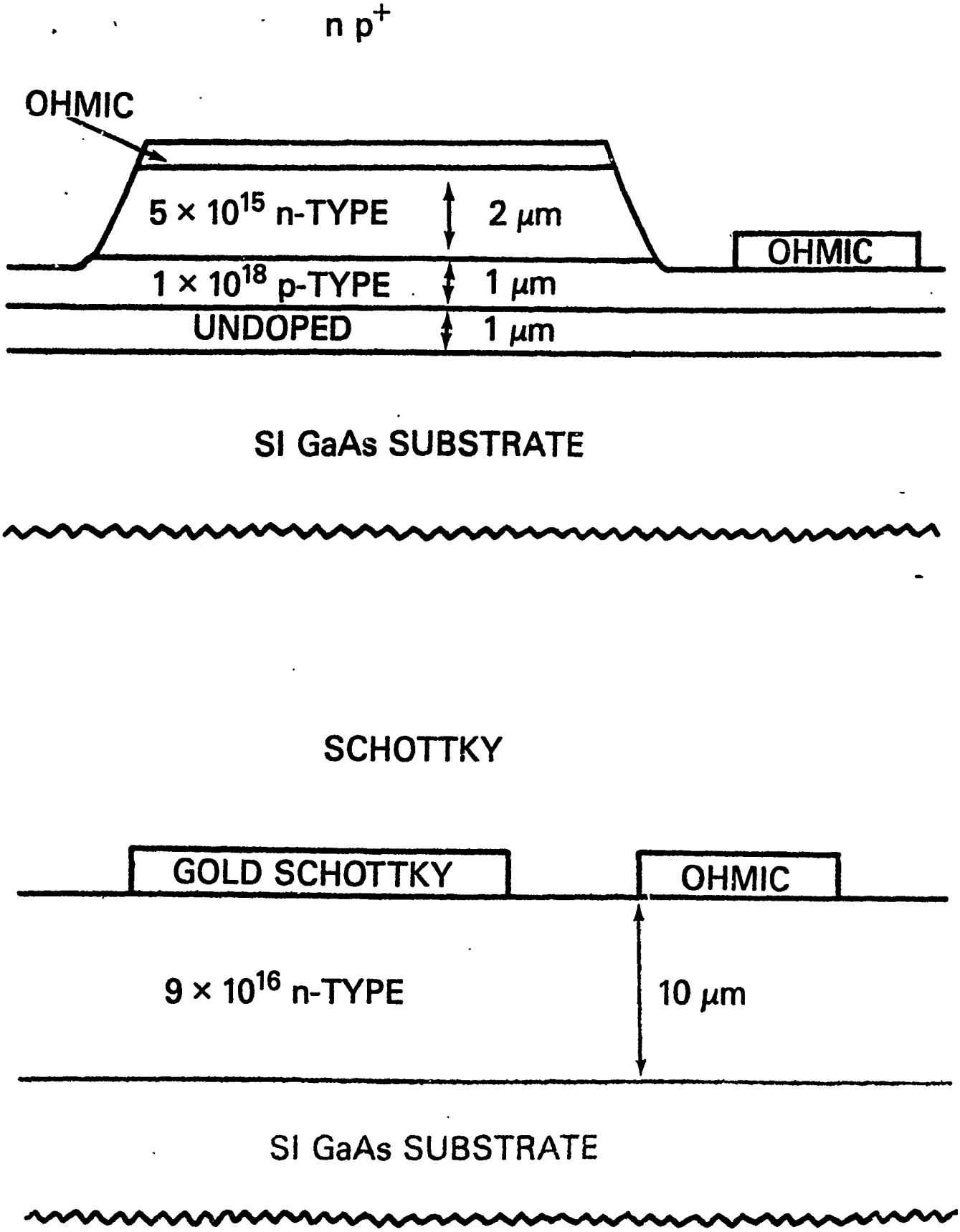
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Fig. 1

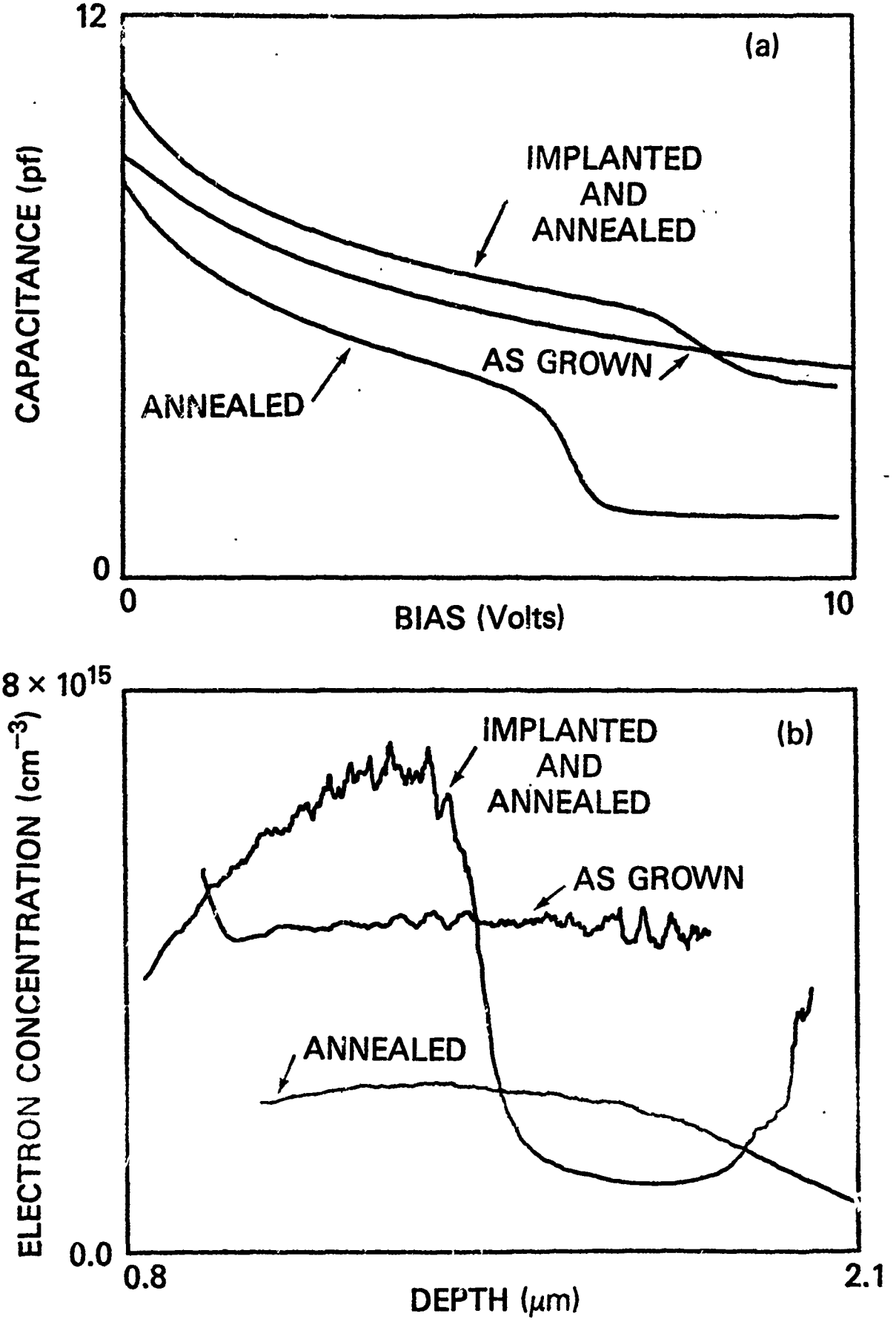
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Fig. 2

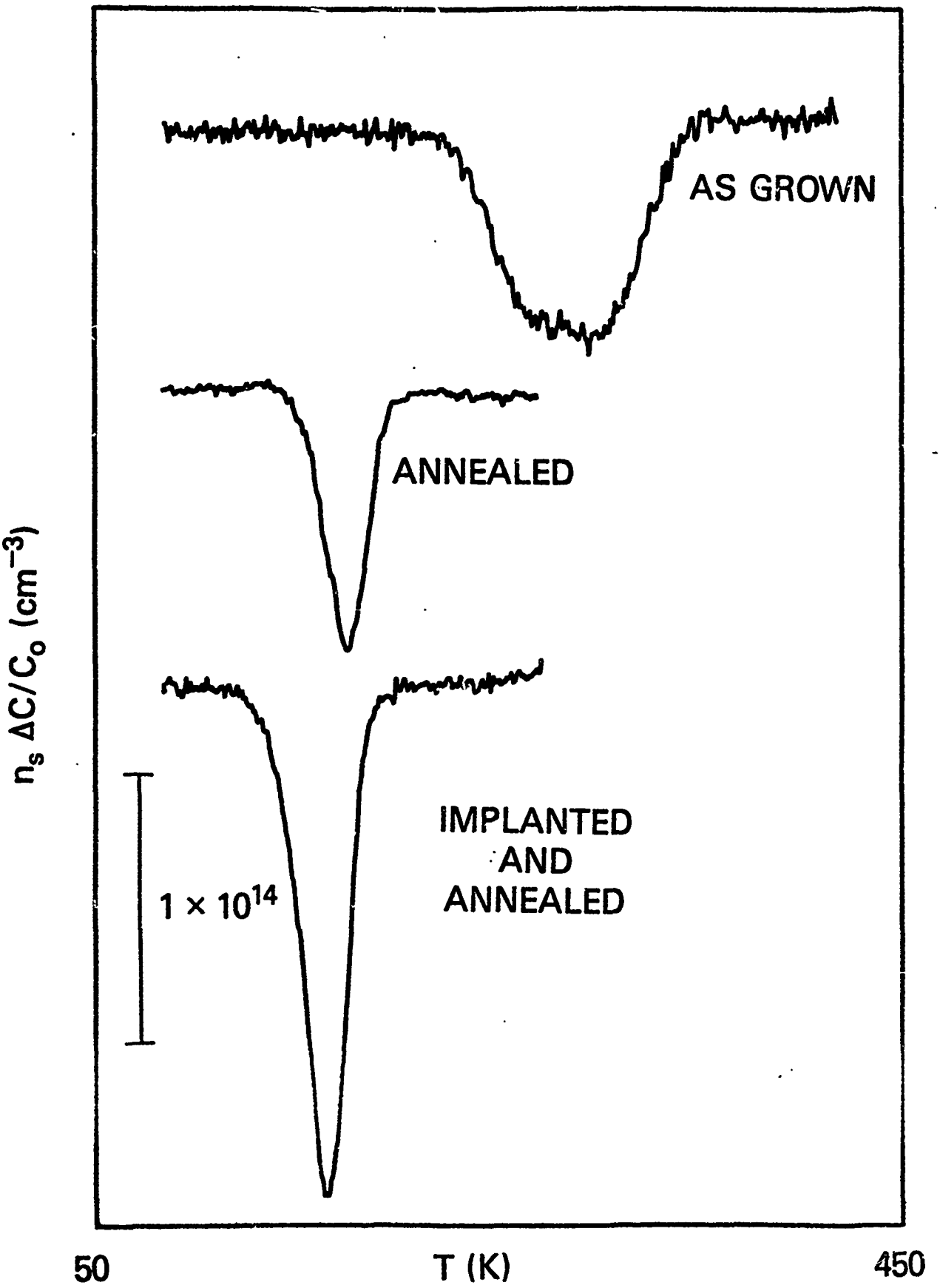
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Fig. 3

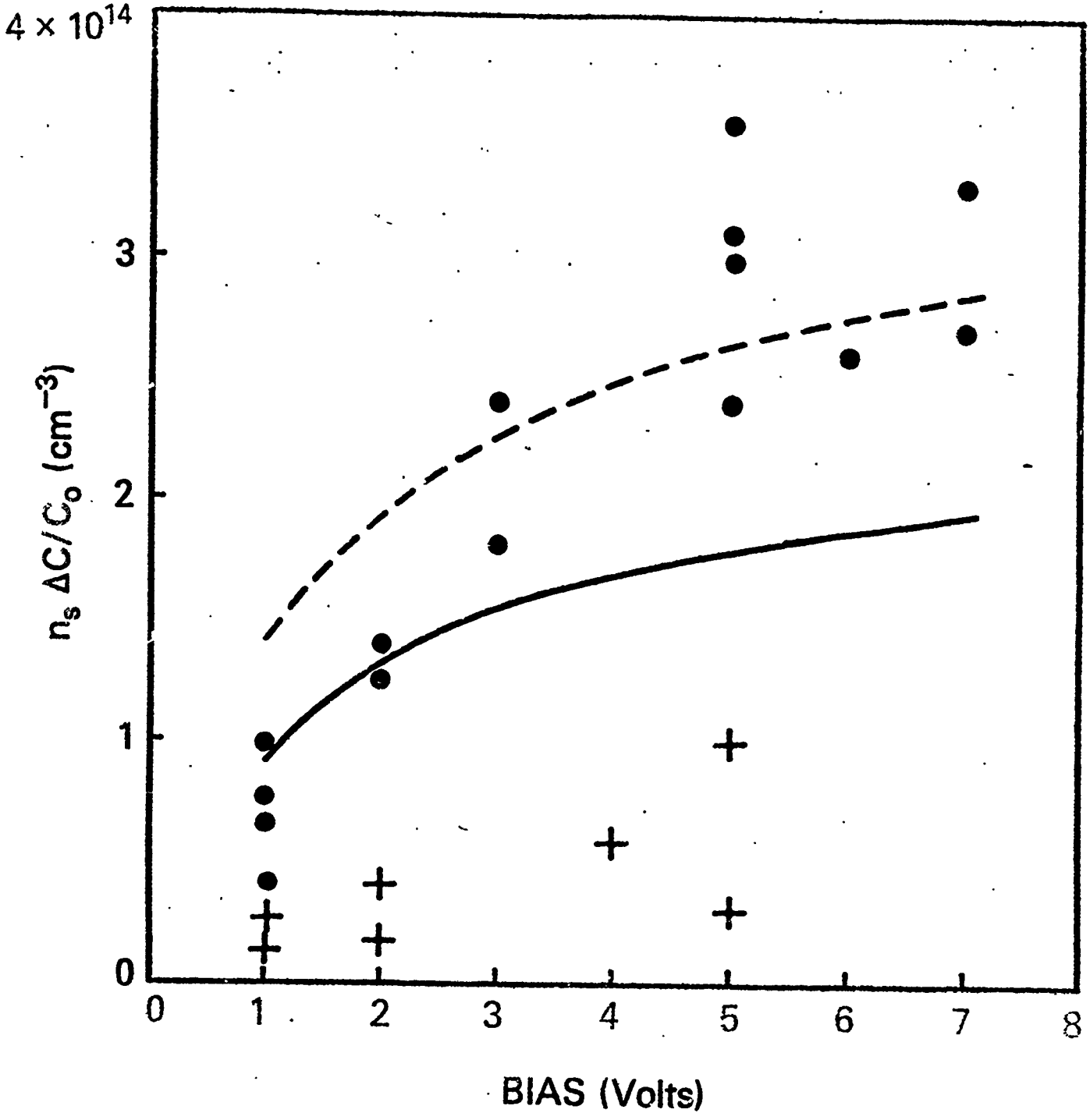
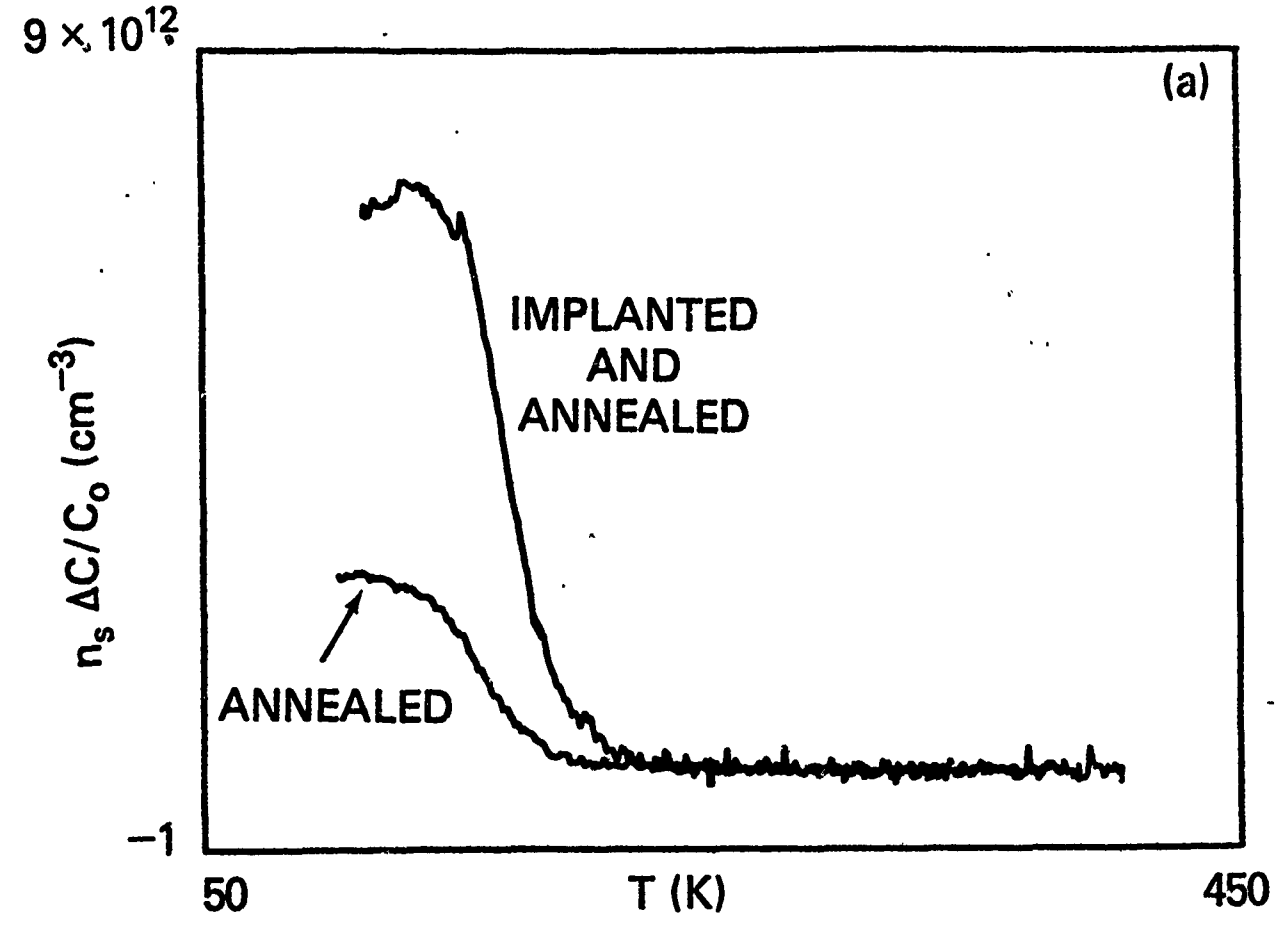


Fig. 4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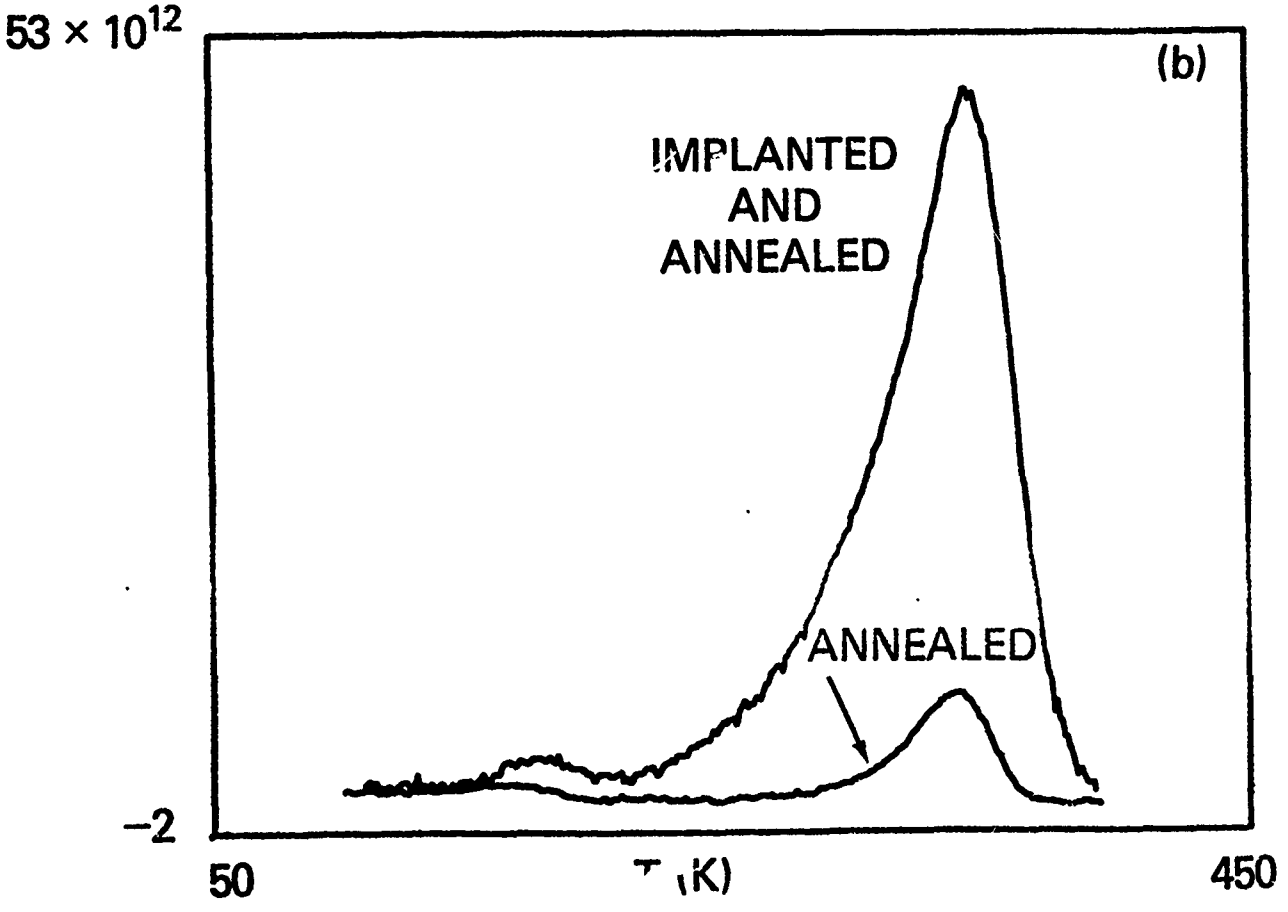
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−2
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Fig. 5

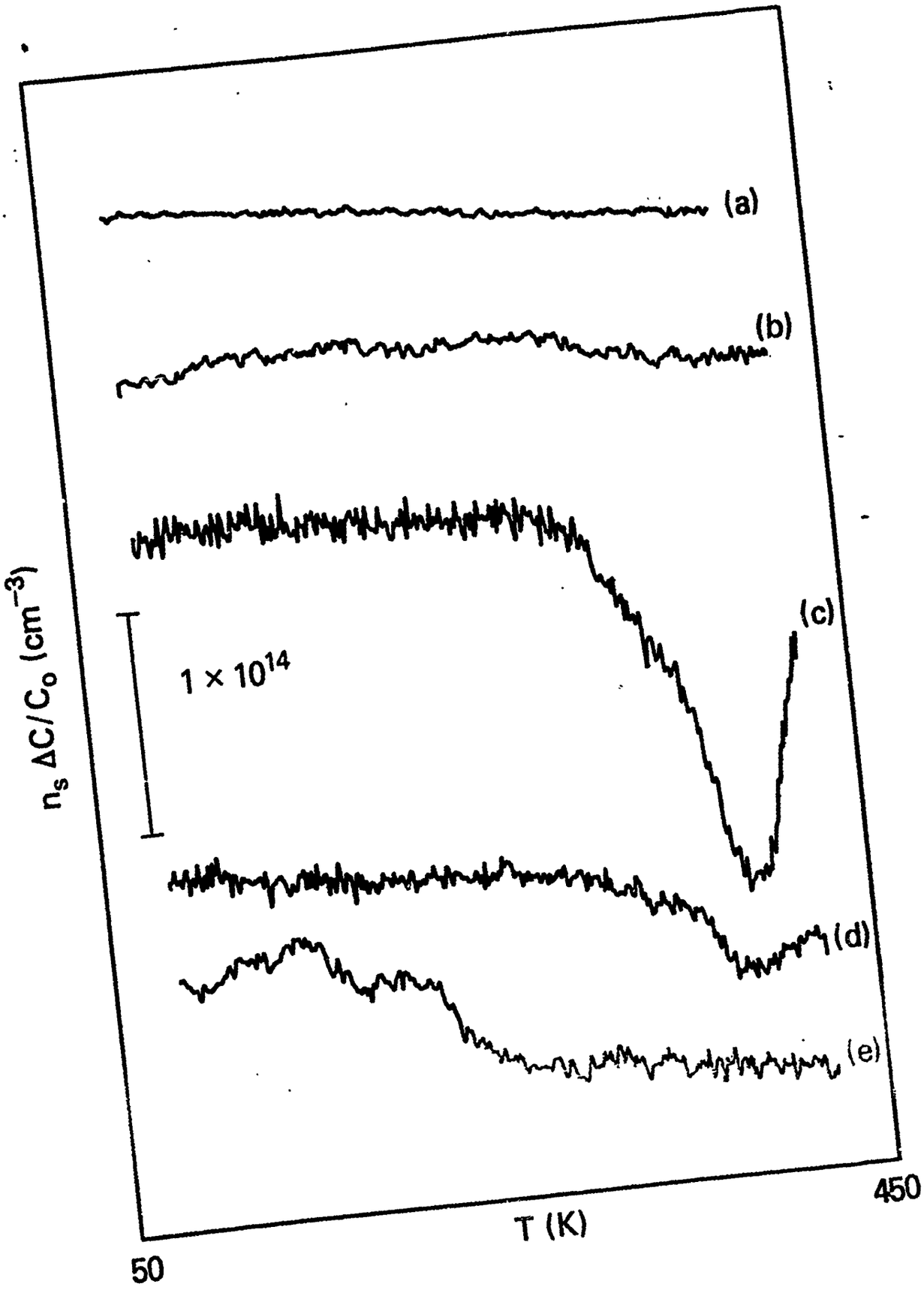

Fig. 6

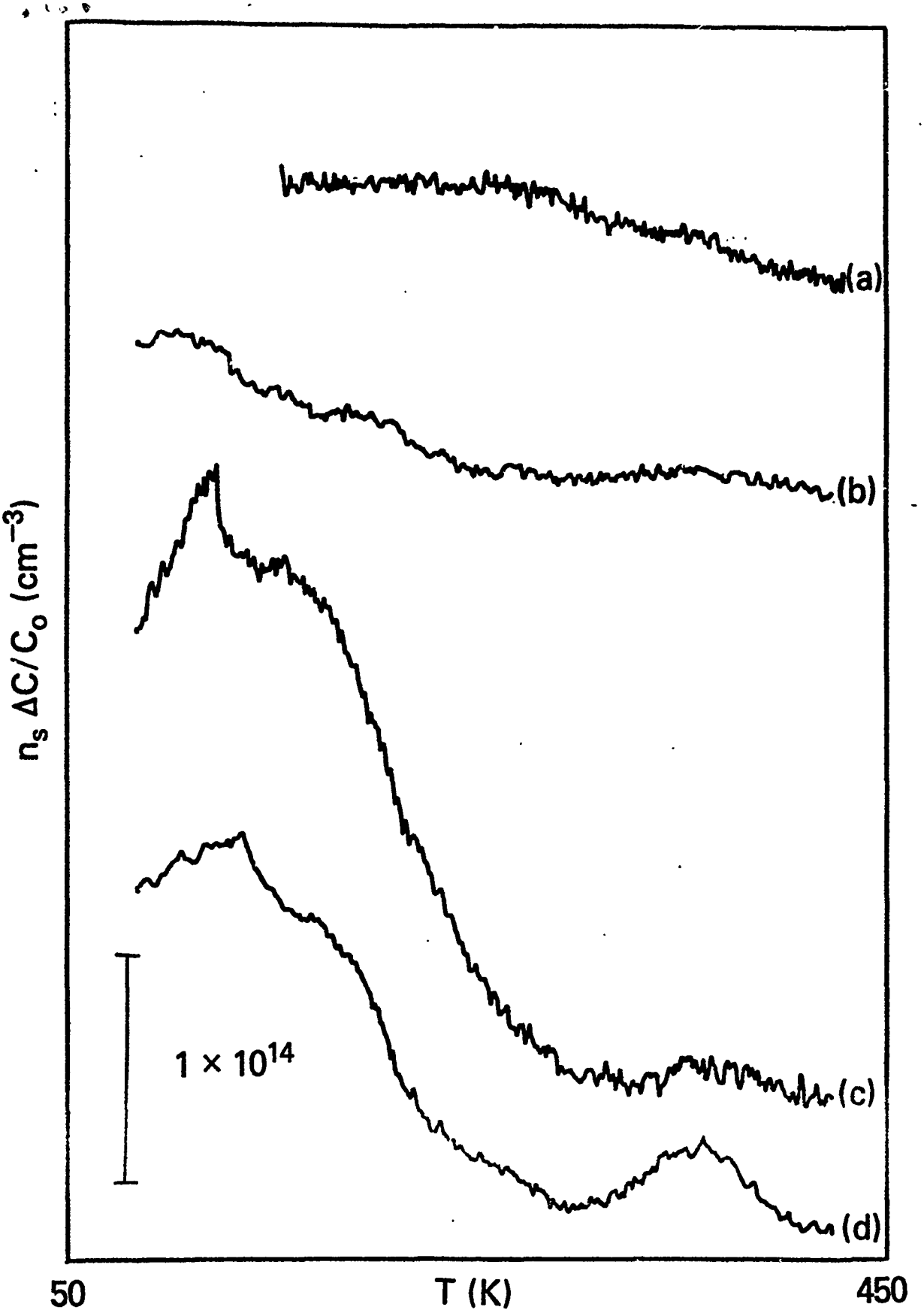

Fig. 7